METHODS FOR GENERATING OUTPUT CONTROL SIGNALS IN SYNCHRONOUS SEMICONDUCTOR MEMORY DEVICES AND RELATED SEMICONDUCTOR MEMORY DEVICES

Abstract

A synchronous semiconductor memory device includes an output control signal generating circuit that generates a data output control signal in response to an internal clock signal, an output control clock signal and a CAS latency signal. The output control signal generating circuit successively shifts read information signals in response to the internal clock signal and the output control clock signal, both source clocks of which are identical, and generates one of the shifted read information signals as an output control signal for indicating a data output period in response to the CAS latency signal. The synchronous semiconductor memory device can synchronize the source clocks of the clock signals used in the output control signal generating circuit thereby reducing the influence of clock jitter.

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